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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/651,944	08/31/2000	Oleg Drapkin	ATI-000152BT	3407

25310 7590 05/12/2005

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EXAMINER	
NGUYEN, HIEP	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 05/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/651,944	DRAPKIN ET AL.
	Examiner	Art Unit
	Hiep Nguyen	2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5,6,8,9,12,13,18,25 and 28-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,6,8,9,12,13,18,25 and 28-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *attachment (5,808,488)*.

DETAILED ACTION

This is responsive to the amendment filed on 03-09-05. Applicant' arguments with respect to reference Bruccoleri (US Pat. 5,808,488) have been carefully considered but they are not deemed to be persuasive to overcome the reference. Thus, the claims remain rejected under Bruccoleri. However, New ground of rejections necessitated by the amendment and new claims is set forth below.

Claim Objections

Claim 28 is objected to because of the following informalities: the recitation " said circuit" in claim 28 lack antecedent basis. It is not clear what is the "said circuit" in the drawing. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 33, 34 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and/ or clarification is required.

Regarding claims 33 and 34, the recitation "...responsive to a rate of change of voltage ..." on line on line 4, "rate of change of a negative edge..." on line 8, 9 in claim 33; "a rate of change of the voltage detection circuit coupled to said input" on line 4, " a rate of change of voltage of a positive edge..." on line 9 in claim 34 are indefinite because they are misdescriptive. None of the drawings shows that the claimed circuit is a slew rate detector i.e., dv/dt detection. The circuits of the present application merely response to the level of the input signal during rising/falling time. The recitation "responsive to a rate of change of voltage of a positive edge of said input signal" is indefinite for the same reason. The circuit only detects the level of the rising or falling input signal. It is inherent that when

any input signal changes from low to high or high to low with **a rate** (slew rate dv/dt or – dv/dt) . The value of the slew rate depends on the structure of the circuit.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 5, 6, 8, 9, 12, 13, 18, 25 and 28-36 are rejected under 35 U.S.C. 102(b) as being anticipated by Bruccoleri et al. (US Pat. 5,808,488).

Regarding claims 1, 2, 18 and, figure 3 of Bruccoleri shows a method for reducing distortion of a signal to and input of an input/output device having parasitic capacitance (Cin) between said input and ground, comprising the step of:

detecting at said input a direction of change in voltage of the input signal applied to the input of inverter (INV1);

introducing a current to the parasitic capacitance to compensate for current of said input signal charging said parasitic capacitance responsive to detection of a positive edge of said input signal. Note that when the input signal voltage rises the parasitic capacitor (Cin) forming by the gate-source/drain of the transistor(s) of inverter (INV1) starts to be charged. When a rising edge of the input signal is detected to be higher than the input threshold, the output voltage of inverter (INV1) becomes low and the output of inverter (INV2) becomes high thus a current is introduced by the output of inverter (INV2) to the parasitic capacitor (Cin) to "compensate" for current of the input signal that charges the parasitic capacitor (Cin). The parasitic capacitance (Cin) exists across the input and the ground. The detection circuit comprises inverter (INV1) and the correction circuit is inverter (INV2). The levels of the input signal are detected at the input of inverter (INV1). When the output of inverter (INV2) is high, a current will flows from the gated power supply (Vdd) to the input (A).

Regarding claims 3 and 19, figure 3 of Bruccoleri shows a method for reducing distortion of a signal applied to an input of a circuit having a parasitic capacitance between said input and ground, comprising the steps of:

detecting at the input (Z+) of said circuit a direction of change in voltage of said input signal; and

preventing discharge of said parasitic capacitance into the input of said circuit responsive to detection of a negative edge of said input signal. Note that when the input (Z+) is low (negative edge), the output of the correction circuit (INV2) is low thus, the parasitic capacitance is discharge via inverter (INV2) and the discharge of said parasitic capacitance into the input of said circuit is prevented.

Regarding claims 5, 6, 25 and 30, figure 3 Bruccoleri shows an apparatus for reducing distortion of a signal applied to an input of a circuit operating at high frequency and having a parasitic capacitance (Cin) between said input and ground, comprising:

a detection circuit (INV1) coupled to said input for detecting a change in voltage of said input signal (Vin+) coupled to said input; and

a correction circuit (INV2) coupled between said detection circuit and said input for compensating for current from said input signal diverted to said parasitic capacitance due to a positive edge of said input signal. It is inherent that the detection circuit (INV1) includes a capacitance directly connecting to one terminal of the parasitic capacitance.

Regarding claims 8, 9 and 31, figure 3 Bruccoleri shows an apparatus for reducing distortion of a signal applied to an input of a circuit operating at high frequency and having a parasitic capacitance (Cin) between said input and ground, comprising:

a detection circuit (INV1) coupled to said input for detecting a change in voltage of said input signal coupled to said input; and

a correction circuit (INV2) coupled between said detection circuit and said input for compensating for current from input signal due to a negative edge of said input signal. It is inherent that the detection circuit (INV1) includes a capacitance directly connecting to one terminal of the parasitic capacitance.

Regarding claims 12 and 13, figure 3 Bruccoleri shows a method for reducing distortion of a signal applied to an input of a circuit having a parasitic capacitance between said input and ground, comprising the steps of:

detecting at said input a direction in change (high or low) in voltage of said input signal;

and introducing a current from the output of the detection circuit (INV2) to said parasitic capacitance to compensate for distortion of said input signal due to said parasitic capacitance responsive to detection of a positive edge of said input signal. When the edge of the input signal is negative, the circuit prevents introduction of a current from the parasitic capacitance into the input signal.

Regarding claims 28 and 29, the detection (tracking) circuit (INV1) is isolated from the output (Vout+) by element (BF1).

Regarding claims 32 and 34, device (INV1) detect the "rate of change of voltage" from low to high. The current generator (INV2) introduces a current to the parasitic capacitance (Cin) to prevent the parasitic capacitance from drawing current from the input signal.

Regarding claim 33, with the negative edge of the input signal i.e., the input signal goes low, the output of circuit (INV2) goes low thus providing a current for preventing discharge of the parasitic capacitance. It is inherently that circuit (INV2) comprises transistors.

Regarding claims 35 and 36, it is well known that inverter (INV2) comprises two transistors (PMOS and NMOS) connected in cascode. The transistor that is coupled to power supply (Vdd) is a current source (see US Pat. Fig.1).

Claims 1-3, 5, 6, 8, 9, 12, 13, 18, 25 and 28-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Hemdal et al. (US Pat. 5,999,042).

Regarding claims 1, 2, 18 and, figure 3 of Hemdal shows a method for reducing distortion of a signal to and input of an input/output device having parasitic capacitance inherently existed between said input and ground, comprising the step of:

detecting at said input a direction of change in voltage of the input signal applied to the input of amplifier (A2);

introducing a current to the parasitic capacitance to compensate for current of said input signal charging said parasitic capacitance responsive to detection of a positive edge of said input signal. Note that when the input signal voltage rises the parasitic capacitor forming by the gate-source/drain of the transistor(s) of amplifier (A2) starts to be charged. When a rising edge of the input signal is detected to be higher than the input threshold, amplifier (A2) starts to amplify the input signal. Current (I2) flows to the negative input of the amplifier and prevent the parasitic capacitance from drawing current from the input signal.

Regarding claims 3 and 19, figure 3 of Hemdal shows a method for reducing distortion of a signal applied to an input of a circuit having a parasitic capacitance between said input and ground, comprising the steps of:

detecting at the negative input of said circuit a direction of change in voltage of said input signal; and

preventing discharge of said parasitic capacitance into the input of said circuit responsive to detection of a negative edge of said input signal.

Regarding claims 5, 6, 25 and 30, figure 3 Hemdal shows an apparatus for reducing distortion of a signal applied to an input (negative) of a circuit operating at high frequency and having a parasitic capacitance between said input and ground, comprising:

a detection circuit (A2) coupled to said input for detecting a change in voltage of said input signal coupled to said input; and

a correction circuit (C7) coupled between said detection circuit and said input for compensating for current from said input signal diverted to said parasitic capacitance due to a positive edge of said input signal. The correction circuit (C7) includes a capacitance (C7) directly connecting to one terminal of the parasitic capacitance.

Regarding claims 8, 9 and 31, figure 3 Hemdal shows an apparatus for reducing distortion of a signal applied to an input of a circuit operating at high frequency and having a parasitic capacitance between said input and ground, comprising:

a detection circuit (A2) coupled to said input for detecting a change in voltage of said input signal coupled to said input; and

a correction circuit (C7) coupled between said detection circuit and said input for compensating for current from input signal due to a negative edge of said input signal. It is inherent that the detection circuit (C7) includes a capacitance directly connecting to one terminal of the parasitic capacitance.

Regarding claims 12 and 13, figure 3 Hemdal shows a method for reducing distortion of a signal applied to an input of a circuit having a parasitic capacitance between said input and ground, comprising the steps of:

detecting at said input a direction in change (high or low) in voltage of said input signal;

and introducing a current from the output of the detection circuit (A2) to said parasitic capacitance to compensate for distortion of said input signal due to said parasitic capacitance responsive to detection of a positive edge of said input signal. When the edge of the input signal is negative, the circuit prevents introduction of a current from the parasitic capacitance into the input signal.

Regarding claims 28 and 29, the detection circuit (C7) is isolated from the output by element (C8).

Regarding claims 32 and 34, device (A2) detects the "rate of change of voltage" from low to high. The current generator (C7) introduces a current to the parasitic capacitance to prevent the parasitic capacitance from drawing current from the input signal.

Regarding claim 33, with the negative edge of the input signal i.e., the input signal goes low, the output of circuit (A2) goes high thus providing a current for preventing discharge of the parasitic capacitance.

Response to argument

In the Remarks, page 13, the Applicant argues that the circuit of figure 3 of Bruccoleri does not operate as teach a method for reducing distortion of a signal to an input /output device having parasitic capacitance between said input and ground. Figure 3 of Bruccoleri shows a flip-flop that has an operation similar to the flip-flop of figure 3 of the present application. The circuit of Bruccoleri **comprises a detection circuit (see attached paper) including inverters (INV1, INV2) and switches (S3, S4) for supplying power to**

the detection circuit when both switches are closed with clock (Vck/). The other elements of the circuit of Bruccoleri are excluded. When both switches (S3, S4) are closed and a rising edge of a signal is applied to the input node (A) of the circuit, the parasitic capacitance (Cin) is charged and a current will flow through the parasitic capacitance. When the input signal applied to none (A) reaches to a level higher than the threshold of inverter (INV1) the output of inverter (INV2) which has a high level is fedback to input node (A). With this high level applied to capacitor (Cin) capacitor (Cin) is fully charged and stops conducting current thus, the distortion of the input signal is reduced. In conclusion; Bruccoleri fully teaches all the limitations of the present invention. Note that the detection circuit of Brucoleri functions with a **switched power supply controlled by switches (S3, S4)**.

The Applicant also argues that "the inverters IV1 and IV2 do not see positive or negative edges of the input signal but to the contrary, see an constant voltage signal". In fact the detection circuit of Bruccoleri receives variable signal so that the parasitic capacitance (Cin) is charged when the input signal change from low to high. The circuit of Bruccoleri will be inactive with a constant input signal. Thus, applying a constant voltage is not a practical way to operate the circuit of Bruccoleri. The Applicant is invited to see figure 1 of Kepler (US Pat. 5,844,836) that is similar to the circuit of Bruccoleri but having fixed supply voltage applied to.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen
05-10-05

TUAN T. LAM
PRIMARY EXAMINER

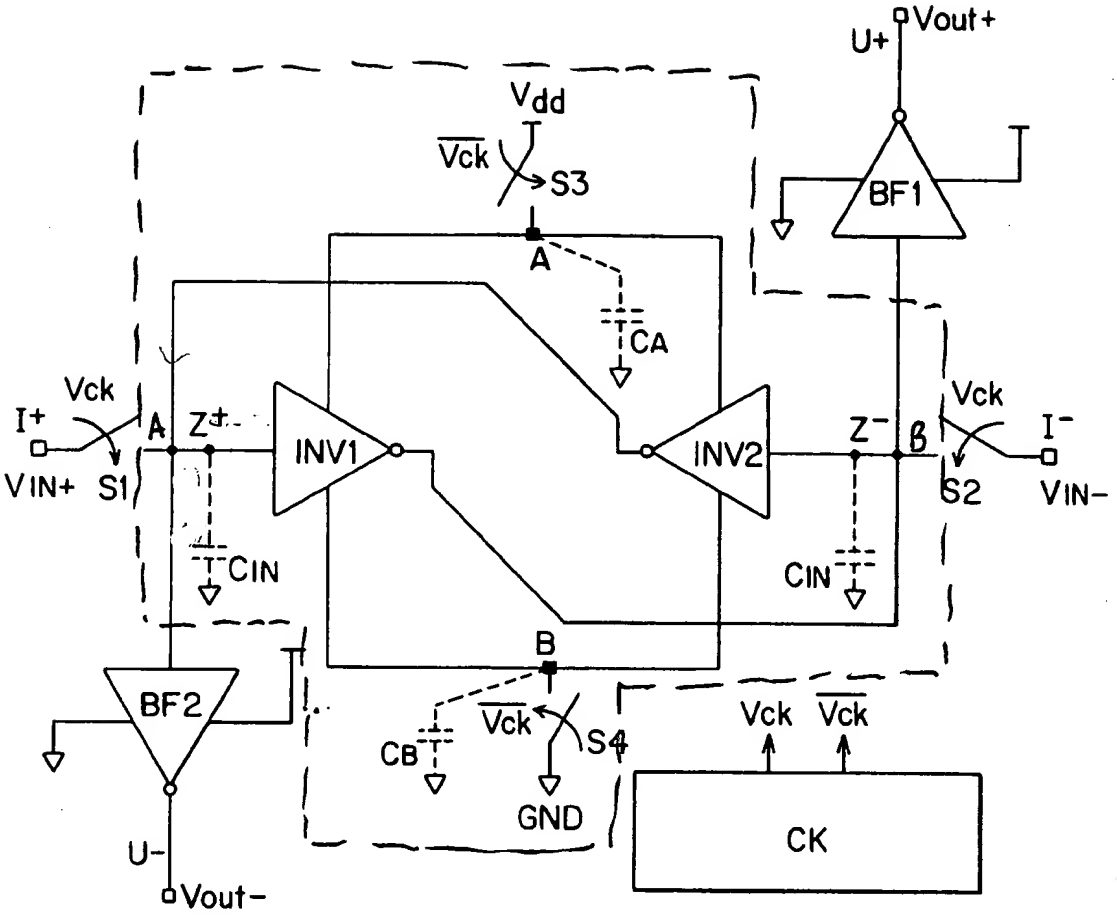

FIG. 2
(PRIOR ART)